REMARKS

Claims 2-5 and 7-9 remain in this application. Claims 1 and 6 have been previously cancelled. Claims 2, 5, 7 and 8 have been amended. Claims 3 and 4 have been previously presented.

Applicants thank the Examiner for the detailed study of the application and prior art.

Applicants have amended the claims to correct the claim objections as indicated on page 2 of the detailed action.

Applicants submit a Request for Continued Examination (RCE) to have this After Final Amendment considered and entered by the Examiner to place the case in condition for allowance.

Also, Applicants have amended each independent claim to recite the processor (for example, a microprocessor) operatively connected to the security key memory. This processor scrambles the contents of the security key memory. Also, the processor resets the single-bit memory device in response to an intrusion such that the security key must be rewritten in the memory.

As to the cited U.S. Patent No. 6,292,898 to Sutherland used by the Examiner to again reject claims as anticipated, Applicants note that Sutherland does not disclose the use of any processor and actually teaches against the use of a processor because as noted in the teachings of the

patent, for example, even in the abstract, active erasure as used by Sutherland enables data to be rapidly erased without requiring the use of a microprocessor and, in some cases, additional devices to effect the erasure or other destruction of data, which use is relatively complex and expensive and does not guarantee destruction of data in situations in which insufficient power may be available to operate the processor.

The claimed electronic signal processing apparatus as now claimed is opposite from Sutherland because as claimed, the apparatus uses a processor when Sutherland, in fact, does not use any processor and teaches against its use. The claimed apparatus also uses a processor in a different manner as compared to prior art uses because the processor operates in conjunction with the single-bit memory device and the security key memory and is configured to issue a reset to the single-bit memory device such that the security key must be rewritten into memory and the processor scrambles the contents of the security key memory. This is opposite from what Sutherland is trying to solve as a technical problem by eliminating the use of a processor.

Not only does Sutherland not anticipate the claimed electronic signal processing as now set forth in this After Final Amendment, but Sutherland teaches opposite.

Applicants contend that the present case is in condition for allowance and respectfully requests that the Examiner issue a Notice of Allowance and Issue Fee Due.

In re Patent Application of:
WALLACE ET AL.
Serial No. **10/764,770**
Filing Date: **January 26, 2004**

If the Examiner has any questions or suggestions for placing this case in condition for allowance, the undersigned attorney would appreciate a telephone call.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: **MAIL STOP AF, COMMISSIONER FOR PATENTS, P.O. BOX 1450, ALEXANDRIA, VA 22313-1450**, on this 18th day of June, 2008.

Julie Lalan